Multicarrier PLC Modem: Novel approach to Data Transmission over Medium-voltage Power Distribution Lines

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Abstract

The paper introduces a novel concept of the PLC modem based on FDM technique with sixteen subcarriers as the alternative product to mainstream PRIME standard using OFDM technique. Medium-voltage or high-voltage power lines represents transmission channels with low frequency selectivity and slow fading. FDM exhibits low processing latency and low PAPR too. This property is especially important for high power amplification that serves to long-range transmission over distribution power lines and makes FDM technique more suitable in comparison with OFDM.

Index Terms

Multicarrier Modulation (MCM), Frequency Division Multiplexing (FDM), Orthogonal frequency-division multiplexing (OFDM), Peak-to-Average Power Ratio (PAPR), Quadrature amplitude modulation (QAM), Trellis Coded Modulation (TCM), Soft-output Viterbi Algorithm (SOVA) with Fixed Lag (FL), Serially Concatenated Convolutional Codes (SCCC), Iterative Decoding Network (IDN), Multipath Propagation, Frequency Selective Channel, Slow Fading Channel, Multiple-Input Multiple-Output (MIMO), Polynomial Singular Value Decomposition (PSVD), Powerline / Cable Point2Point / Point2Multipoint Communication, Carrier Sense Multiple Access (CSMA), Time Division Multiple Access (TDMA), Field Programmable Gate Array (FPGA), Digital signal processor (DSP, Powerline Intelligent Metering Evolution (PRIME).

I. Introduction

THERE are two essential techniques of multipath propagation suppression. The first technique is OFDM based on integral transformation with complex exponential core. This frequently used technique has extreme resistance to multipath propagation and it is applied in the PRIME standard. An OFDM technique is also characterized by high spectral efficiency that grows with number of overlapping subcarriers or with duration of OFDM symbol if you like. The overall bandwidth of OFDM modulation is divided to many narrow subbands that causes incredible resistance for channel frequency selectivity, because channel coherence bandwidth is often much higher then subband width. On the other hand, the OFDM technique has block oriented processing. With the growth of the number of carriers also growing duration of OFDM symbol and a proccessing latency in the integral transformations of the transmitting and receiving side. Moreover, the consequent blocks have to be separated from each other by guard intervals (cyclic prefixes). Otherwise multipath propagation causes mixing (fusion) of this blocks and malfunction of detection. The cyclic prefixes are requisite staffage that is useless for user data transmission and occupy the line. Of course, the length of cyclic prefixes must to be longer than channel correlation time (difference between the delay of the first and last propagation path). The last significant disadvantage rests in huge PAPR that makes difficult the appropriate power amplification for long-range transmission and also makes the high power amplifier more expensive.

The second technique is common FDM based on the set of complex mixers that are attached to the outputs of linear or nonlinear narrowband modulators. The distribution of subcarriers along the overall FDM modulation bandwidth is arbitrary and bandwidths of particular subbands are arbitrary too. Spectral efficiency of FDM is generally less as in the case of OFDM and immunity to the multipath propagation is worse too. On the other hand, the FDM technique do not use integral transformation and can be processed continuously without significant latency. Cyclic prefix insertion is not required and link capacity is disengaged for user data. Also the PAPR is lower that is important for effective power amplification and long-range transmissions.

As was said in the abstract the power lines are long-range transmission channels with relative rigid frequency characteristic. Therefore we suppose the FDM is more suitable for such applications, because the main OFDM advantage is not needed.

II. Product overview

Our approach is based on the frequency division multiplexing of narrowband linear digital modulations using square root raised cosine modulation impulse with roll-off factor 0.4 and constellation QPSK. Overall bandwidth is assumed 96 kHz and it is divided to 16 subchannels centered on frequencies 30, 36, 42, 48, 54, 60, 66, 72, 78, 84, 90, 96, 102, 108, 114 and 120 kHz. Subchannel bandwidth is 5.5 kHz. Two different channel coding will be included. The essential trellis coding (TCM) as well as advanced serial turbocode (SCCC) and iterative detection (IDN) that will be applied in future versions. The two different trellis encoders with code ratio 1/2 will be available. The feedforward 1st order (two states) binary code and feedback 2nd order (four states) binary code. Approach contains a flexible thread allocation unit that allows arbitrary merging of subchannels for particular user data streams. Each subband can serve to one slow data stream or all subbands can be joint together for one fast data stream. Of course, the arbitrary transmission scenario that lying between both mentioned boundary scenarios is possible.

Modular design allows easy adaptation for many purposes. Mounting in standardized DIN rails makes integration into existing systems easy. Seamless interconnection between modem and computers or sensors is guaranteed.

The primary area of use is smart grid networking transmissions in high voltage (10 kV to 35 kV) power lines and for transmissions in hostile environments (especially in cables that was not originally designed for communication purposes). Network topology is assumed as POINT2POINT, POINT2MULTIPOINT with master/slave management based on CSMA or TDMA. Other areas of our concept usage are Internet of Things, Controlling of power distribution grid, Optimization of power distribution grid, Automatic Meter Reading (AMR), Billing, Anti-theft monitoring, Remote controlling, Advanced Metering Management (AMM) and Advanced Metering Infrastructure (AMI).

III. Hardware design

The prototype hardware platform contains two fundamental processing units. The FPGA unit (Altera Cyclone III) and the DSP unit (ARM microcontroller). The FPGA is reserved only for physical layer and DSP serves to the link layer processing and networking features. Both units (layers) are connected by wide data bus. Data transmission between layers is performed in burst mode. Firmware is divided into two sets for each unit. Source code for physical layer is being developed in Verilog HDL and source code for link layer in C language.

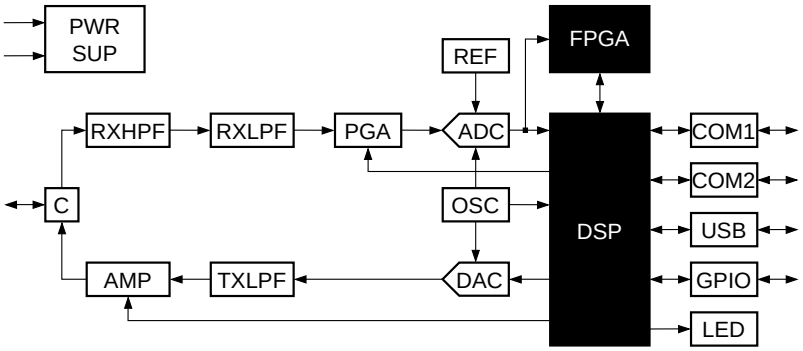

Fig. 1: Modem block diagram.

The analog part of platform is ordinary and compounded of two branches. Both cascades are binded by the Rx/Tx combiner/splitter (C). The receiving cascade starts by pair of complementary filters. The first one is active 6th order low-pass filter (RXLPF) and the second is active 2nd order high-pass filter (RXHPF). Noise and interference free signal is consequently amplified to appropriate power level by the amplifier (PGA) with programmable gain directed from DSP.

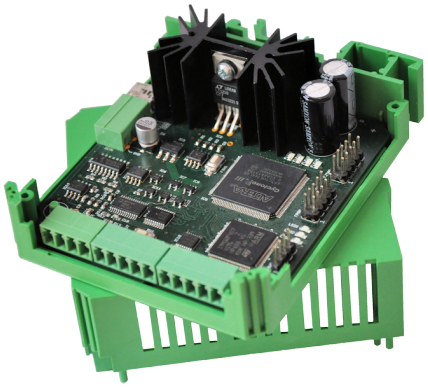

Fig. 2: Side view.

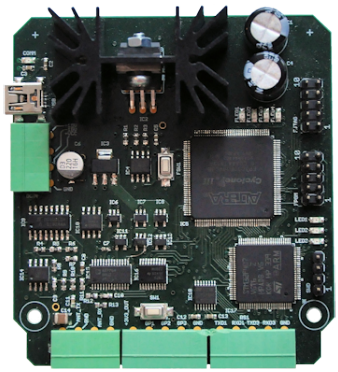

Fig. 3: Top view.

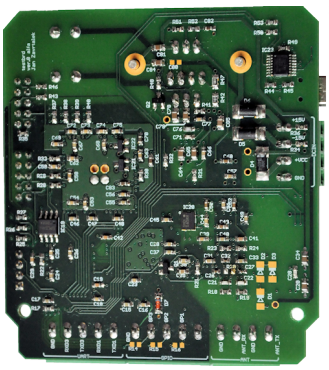

Fig. 4: Bottom view.

The receiving cascade ends by the analog to digital converter (ADC) controlled by the clock generator (OSC) and voltage reference (REF). The transmitting cascade starts by digital to analog converter (DAC). The analogue signal is consequently smoothed by anti-image active 2nd order low-pass filter (TXLPF) and amplified in the power amplifier (AMP). External communication is ensured by the couple of serial ports RS-232 (COM1 and COM2) and by the one USB port (USB). The block of digital input/output for external equipment (GPIO) is also present as well as LED color indicators for diagnostic purposes. The sampling frequency is 250 kHz, (-3 dB) bandwidth is 3-150 kHz and RMS/Peak output power is 9W/29W. Power consumption of receiving is 3W. The mounting box has 45 mm in width and has IP20.

IV. Physical layer

The first L1 firmware (alpha version) was released in August 2016 and contains complete L1 without channel encoders and decoders. Alfa version is divisible to the transmitting front-end, receiving front-end, channel synchronizer, frame synchronizer and soft-output demodulator (SODEM). The transmitting front-end contains cascade of pulse shaping filter (interpolation FIR filter), linear interpolator (2nd up-sampling), up-converter (complex mixer with numerically controlled oscillator), rf signal buffer (summation of signals from active subbands) and step amplifier that amplify resulting rf signal to desirable (same) level with respect to number of active subbands. The recieving front-end is complementary unit to the transmitting front-end and contains rf signal buffer followed by down-converter (complex mixer with numerically controlled oscilator) and down-sampling cascade of three decimation FIR filters. The receiving front-end is the complementary unit to the transmitting front-end and contains rf signal buffer followed by down-converter (complex mixer with numerically controlled oscillator) and down-sampling cascade of three decimation FIR filters. Obtained uder-sampled baseband signals of particular subbands are consequently synchronized in channel synchronizer that contains three subblocks. The first one is the automatic gain control (AGC), second one is the complex Costas loop and last one is the phase ambiguity domain synchronizer. The AGC stabilize differently attenuated complex envelopes of particular subbands to unified level required by Costas loops, because it is desirable that all loops converge with same speed on average. The Costas loops perform fine phase synchronization and ambiguity domain synchronizers makes the final phase rotation to the true phase domain. The synchronized complex envelopes are fed to frame synchronizer where the beginnings of individual user data packets are found as well as correct polyphase component of incoming complex envelopes. The correct polyphase components are consequently transformed to the detector metric in the SODEM. The L1 frame consists of the training (constant) sequence, Legendre's synchronization preamble of length 31 symbols with a cyclic prefix of length 1 symbol, user data packet and the termination token (couple of Legendre's synchronization preambles). The training sequences serve to stabilization of Costas loops and to phase ambiguity removal. Legendre's sequence is used to frame synchronization based on pair of correlators (binary and fine).

The second L1 firmware (beta version) is assumed to be released in December 2017 and will contain also trellis encoders and decoders as well as thread allocation unit on the transmitting side and thread deallocation unit on the receiving side. As the decoding algorithm was chosen Soft-output Viterbi algorithm with Fixed Lag [1](FL-SOVA) because provide good performance with relatively low computational and memory requirements.

System variant	Packet length [bits]	Preamble length [bits]	Alphabet	Subchannel bitrate [kbit/s]	Modulation bitrate [kbit/s]	User data bitrate [kbit/s]	Usage
Trellis code 1/2 protected	1024	32	QPSK	3.9	62.4	60.5	LOW SNR $>$ 4 dB
	2048	32	QPSK			61.5	
	4096	32	QPSK			61.9	
Uncoded	1024	32	QPSK	7.8	124.8	120.9	HIGH SNR $>$ 10 dB
	2048	32	QPSK			122.9	

TABLE I: Bit rate upperbounds.

V. Link layer

Our concept assumes two network topologies (POINT2POINT, POINT2MULTIPOINT) based on master/slave communication principle and two possible access modes that use half-duplex transmission, proprietary protocol and serial port interface. Starting product will support only CSMA. Consequent releases should make use of TDMA that is much more effective in terms of channel capacity utilization.

VI. Product evolution

There are several ways of the concept evolution. The first direction rests in expansion of common TCM to the layered variant that allow application of constellations with high cardinalities. We suppose application of quadrature amplitude modulation from 16QAM (two layers) to 256QAM (four layers). Of course, this step will require a change of channel synchronization. The Costas loops will have to be replaced by precise data aided synchronizers of phase rotation and symbol timing.

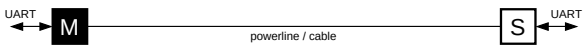

Fig. 5: POINT2POINT Network topology.

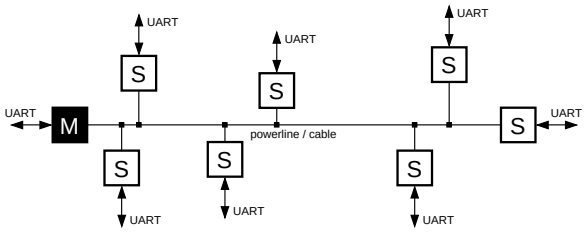

Fig. 6: POINT2MULTIPOINT Network topology.

The second direction rests in addition of serial turbocode (SCCC) and iterative decoding network (IDN). Turbocode have much better performance in comparison with common TCM, but application introduces relative high latency (decoding is iterative) and also requires relatively high consumption of logical elements and memory elements in comparison with FL-SOVA where detection is practically continuous and memory requirements negligible. In the case of QAM constellations is necessary to apply layered variants of turbocodes and iterative decoding networks that are quite complicated and have a higher consumption of FPGA resources.

The third direction rests in reducing of number of transmitting subbands to achieving of lower PAPR and the more effective power amplification. This reduction will require an extension of the channel synchronization by the equalizer. Our company already have prepared effective and hardware-friendly solution using equalization in the time domain by the two-pole autoregressive filtration.

The last direction for distant future rests in application of Multiple-Input Multiple-Output (MIMO) technique with Polynomial Singular Value Decomposition (PSVD).

VII. Conclusion

The novel approach of data transmission over medium-voltage power lines based on FDM technique was introduced as the alternative product to PRIME standard. The prototype of our starting product has been developed and it is prepared for serial production. Also the alpha version of L1 firmware in Verilog HDL is finished and our company now intensively working towards to beta version that is expected to be finished to the end of 2017. The maximum hardware requirements of beta version were upper bound to 10k logical elements and maximum clock frequency is going to be increased to 150 MHz. Hardware requirements and maximum clock frequency of currently developed firmware (alpha version) is summarized in the consequent table. Other product evolution directions have been discussed. Our company already have prepared and examined all scenarios of product evolution through computer simulation and these scenarios are prepared for implementation to real-time working hardware.

Top level entity	Logic elements	Logic registers	Memory bits	Embedded Multipliers	Max. clock freq. [MHz]
Transmitter	788	382	9376	3	101.34 (Model 85C)
Reciever	4054	1954	80096	16	103.06 (Model 85C)

TABLE II: Compilation report of L1 firmware (Alpha version) in Altera Cyclone III.

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